Co-funded by the Erasmus+ Programme of the European Union

SMARTCITY
Innovative Approach Towards a Master Program on Smart Cities Technologies

Mongolian University of Science and Technology
Curriculum development and Registration office

COURSE SYLLABUS

Course name	Semiconductor Integrated Circuit Technology		
Course code	F.EE702	**Course credit**	3
Department	Electronics	**School**	SICT
Pre-requisites Course Code	None	**Co-requisites Course code**	None
Primary instructor	Zagarzusem Khurelbaatar	**Room number**	220
E-mail address	zagarzusem@must.edu.mn	**Phone number**	-
Other instructors	None		
Learning Hours	Total: 144 Learning hours (2:2:0:5) Lecture (32 hr), Seminar (32 hr), Assessment (80 hr)		
Course type	☑ Compulsory ☑Elective ☐ Selected elective ☐ Other		
Terms Offered	☑ 1st Semester ☑ 2nd Semester ☐ Summer ☐ Year Long		

INSTRUCTION LANGUAGE

- Mongolian or English

Learning Sources: (Textbooks, journals, website addresses etc)

Textbooks:

- G. E. Anner, *Planar Processing Primer*, Springer, ISBN: 978-94-009-0441-5, 1990.
- Y. Taur and T. H. Ning *Fundamentals of Modern VLSI Devices*, 2nd Edition, Cambridge University Press, 978-0-521-83294-6, 2015.

Supplemental materials:

- S. M. Sze and M. K. Lee *Semiconductor Devices: Physics and Technology*, 3rd Edition, John Wiley and Sons, ISBN:978-0470-53794-7, 2012.
- C. Hu *Modern Semiconductor Devices for Integrated Circuits*, Pearson/Prentice Hall, 1st Edition. ISBN: 978-0136085256, 2010.

DESCRIPTION OF THE COURSE

The goal of this course is to give advanced undergraduate students a thorough understanding of the design and process technology of modern integrated circuits. Several key aspects including direct hands-on exposure to all aspects of processing technology, experience in the design of semiconductor device processes, and a clear understanding of the economic and technical trade-offs inherent in this industry.

AIMS AND OBJECTIVES OF THE COURSE

This course aims at understanding the manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI chip and nano fabrication. The students will be provided with a completed guide for the semiconductor device design by using the modern CAD tools.

Objectives:

1. Understanding of the modern CMOS technologies
2. Design of semiconductor device process
3. Explain MEMS and NEMS technologies

COURSE CONTENTS, TIME SCHEDULE

Lecture content:	**Hours**
• Introduction, Historical perspective and technology trends.	2
• Modern CMOS technologies: CMOS process flow starting from substrate selection to multilevel metal formation, comparison between bulk and SOI CMOS technologies.	2
• Process integration	2
• Silicon wafer, crystal growth and wafer manufacturing: Crystal structure, Czochralski and FZ growth methods, wafer preparation and specifications, SOI wafer manufacturing.	2
• Clean rooms, wafer cleaning and gettering: Basic concepts, manufacturing methods and equipment, measurement methods	2
• Vacuum technology: Vacuum pumps	2
• Semiconductor computer aided design: Silvaco TCAD	2
• Oxidation: wet and dry oxidation, growth kinetics and models, defects, measurement methods and characterization.	2
• Photolithography: light sources, Wafer exposure systems, Photoresists, Baking and development, Mask making, Measurement of mask features and defects, resist patterns and etched features.	2
• Nanofabrication by Self-Assembly	2
• Etching processes: Wet etching, Plasma etching, RIE, etching of materials used in VLSI, Modeling of etching.	2
• Diffusion technology; Models for diffused layers, Characterization methods, Segregation, Interfacial dopant pileup, oxidation enhanced diffusion, dopant-defect interaction.	2
• Thin film deposition: Physical vapor deposition, epitaxial growth, manufacturing methods and systems, deposition of dielectrics and metals commonly used in VLSI, Modeling deposition processes.	2
• Thin film deposition: Chemical vapor deposition	2
• Ion beam processing: Basic concepts, High energy and ultralow energy implantation, shallow junction formation & modeling, Electronic stopping, Damage production and annealing, RTA Process & dopant activation.	2
• Backend processes: Contacts, Vias, Multi-level Interconnects, Silicided gates and S/D regions, Reflow & planarization, Multi-chip modules and packaging.	2
Seminar content:	**Hours**
• Introduction, Historical perspective and technology trends.	2
• Modern CMOS technologies: CMOS process flow starting from substrate selection to multilevel metal formation, comparison between bulk and SOI CMOS technologies.	2

• Semiconductor economics, process integration	2
• Silicon wafer, crystal growth and wafer manufacturing: Crystal structure, Czochralski and FZ growth methods, wafer preparation and specifications, SOI wafer manufacturing.	2
• Clean rooms, wafer cleaning and gettering: Basic concepts, manufacturing methods and equipment, measurement methods	2
• Vacuum technology: vacuum pumps	2
• Examples of Silvaco TCAD	2
• Oxidation: wet and dry oxidation, growth kinetics and models, defects, measurement methods and characterization.	2
• Photolithography: light sources, Wafer exposure systems, Photoresists, Baking and development, Mask making, Measurement of mask features and defects, resist patterns and etched features.	2
• Nanofabrication by Self-Assembly	2
• Etching processes: Wet etching, Plasma etching, RIE, Etching of materials used in VLSI, Modeling of etching.	2
• Diffusion technology; Models for diffused layers, Characterization methods, Segregation, Interfacial dopant pileup, oxidation enhanced diffusion, dopant-defect interaction.	2
• Thin film deposition: Physical vapor deposition, epitaxial growth, manufacturing methods and systems, deposition of dielectrics and metals commonly used in VLSI, Modeling deposition processes.	2
• Thin film deposition: Chemical vapor deposition	2
• Ion beam processing: Basic concepts, High energy and ultralow energy implantation, shallow junction formation & modeling, Electronic stopping, Damage production and annealing, RTA Process & dopant activation.	2
• Backend processes: Contacts, Vias, Multi-level Interconnects, Silicided gates and S/D regions, Reflow & planarization, Multi-chip modules and packaging.	2

TEACHING AND LEARNING ACTIVITY

Weekly contact hours: (2:0:2:5)-1×2 hours lecture, 1×2 hours laboratory. Traditional and active learning methods will be used within lecture, laboratory and homework assignments

TEACHING METHODS	TYPES OF TEACHING METHOD	CLOs
➢ Problem based	✓ Lecture	1,2,3,4,5,6
➢ Inquire based	✓ Laboratory	7,8,9,10

METHOD OF ASSESSMENT

Assessment tools	Assessment frequency	Weight	CLOs
Attendance/participation in class	Weekly/ Every 3 weeks	8%	1,2,3,4
Assessment	8, 13th week	15%	2,3,4,5,6
Med-term	8, 13th week	15%	1,2,3,4
Laboratory	Every 2 weeks	32%	7,8,9,10
Final exam	17th week	30%	1,2,3,4,9

PREPARED:

Course coordinator	**Kh.Zagarzusem**	**Date:**	**2018/01/10**

BIBLIOGRAPHY

1. G. E. Anner, *Planar Processing Primer*, Springer, ISBN: 978-94-009-0441-5, 1990.
2. Y. Taur and T. H. Ning *Fundamentals of Modern VLSI Devices*, 2nd Edition, Cambridge University Press, 978-0-521-83294-6, 2015.
3. https://dynamic.silvaco.com/
4. http://www.ocw.titech.ac.jp/
5. http://web.iitd.ac.in/~mamidala/id54.htm
6. https://www.pdx.edu/ece/ECE516